Amendments To the Drawings:

The attached sheets of drawings include changes to Figs. 1d(iv), 2b(i), 2b(ii), 4a, 4b, 5a, 5b, 5c, 6a, 6b, 7b, 7c, 8a(i), 10a(i), 10a(ii), 10a(iii), 10b(i), 10b(ii), 10b(iii), 10c, 11a(i), 11a(ii), 11b(i), 11b(ii). 11b(iii). The changes are too numerous to enumerate. No new matter has been introduced. Please replace Figs. 1d(iv), 2b(i), 2b(ii), 4a, 4b, 5a, 5b, 5c, 6a, 6b, 7b, 7c, 8a(i), 10a(i), 10a(ii), 10a(iii), 10b(i), 10b(ii), 10b(iii), 10c, 11a(i), 11a(ii), 11b(i), 11b(ii). 11b(iii) with the attached Replacement Sheets. No new subject matter has been added.

Attachment: Replacement Sheets

REMARKS/ARGUMENTS

A petition and fees for a two-month extension of time are being submitted herewith.

The Abstract has been replaced to conform to the word-count limitation and in proper form. The Amendments to the Specification corrects certain typographical errors. The Amendments to the Figures correct certain drawing errors and inconsistencies. No new matter has been introduced in either of the Amendments.

Claims 1, 5-19, 23-32, and 36-43 remain pending.

Claims 4, 22, and 35 have been cancelled.

Claims 1, 18, 31, and 32 have been amended, as recited hereinabove.

Claims 44 – 45 have been added.

Claims 1, 18, and 31 have been amended and are now believed to overcome the objection made thereto.

Claim 32 has been amended to present language consistent with the other claims.

Claims 1, 4, 6-14, 18-19, 22-32 and 35-43 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA" and Utsunomiya et al. (US Pub.:2003/0131166).

Claim 5 was rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA" and Utsunomiya et al. (US Pub.:2003/0131166) as applied to claims 1, 4, 6-14 and 18-43 above, and further in view of Boucher et al. (US Patent 6,434,620).

Claims 15-16 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA," Utsunomiya et al. (US Pub.:2003/0131166) and "Serial ATA Specification."

Claim 17 was rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA," Utsunomiya et al. (US Pub.:2003/0131166), and Shin et al. (US Patent 7,154,905).

The cited references do not individually teach or disclose each and every element of the claimed invention

GRIEFF:

Grieff does not teach "an arbitration and control circuit … responsive to the original queue depth value and operative to alter the original queue depth value into a queue depth value that is less than the original queue depth value ….", as in the claimed invention. To this end, there is never any overrun problems with the queue encountered where the host units provide more commands than that which can be queued because, in accordance with the claimed invention, the host units are, advantageously, each fooled into thinking the queue depth is smaller than it actually is. This avoids the problem Grieff encounters and recognizes in that its hosts can overrun the queue depth resulting in an error. [See: Grieff: Fig. 2, note on the bottom left-side of the page, starting with "Don't forward the Queued command to the Device if the Task Queue is full. Make it look like the device had an error …."] Advantageously, such an error cannot occur in the claimed invention because the queue will never be overrun.

Further, Grieff does not teach the "… first host task file", "… second host task file", "… device task file", and "an arbitration and control circuit coupled to said first host task file and said second host task file and said device task file for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state …", as recited in claims, 1, 18 and 31.

Utsunomiya:

Utsunomiya does not teach "an arbitration and control circuit … responsive to the original queue depth value and operative to alter the original queue depth value into a queue depth value that is less than the original queue depth value ….", as in the claimed invention.

Further, Utsunomiya does not teach "a first SATA port including a first host task file for connection to a first host unit", "a second SATA port including a second host task file for connection to a second host unit", and "an arbitration and control circuit coupled to said first host task file and said second host task file and said device task file for selecting one of the first host

or second host units to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state …", as recited in claims, 1, 18 and 31. While Utsunomiya discloses a task file queue (in main memory 16) and a task file (in AT drive 12), and neither the task file queue nor the task file are SATA task files, as in the claimed invention. Further, Utsunomiya's task file queue appears to be in the host and not in a host port of a switch, as in the claimed invention. Similarly, the task file of Utsunomiya appears to be in the device (or drive) and not in a port of a switch, as in the claimed invention.

The claimed first and second task files are in the SATA ports responding to corresponding host units, and not host memory, as in Utsunomiya. Even if the main memory of Utsunomiya that houses its task file queue is considered to be a host itself, there is no port, such as in the claimed invention.

While the task file queue is disclosed to accept more than one command, it does so from the same CPU, this is not "selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting non-data FIS, from either of the first or second host units, at any given time, including when the device is not in an idle state …", as in the claimed invention.

Further, in Utsunomiya there is no device task file in a switch, rather, the AT drive 12 is located in the device (or drive).

Ooi '045 and '787:

Neither Ooi '045 nor Ooi '787 do not teach "an arbitration and control circuit … responsive to the original queue depth value and operative to alter the original queue depth value into a queue depth value that is less than the original queue depth value ….", as in the claimed invention.

Furthermore, neither Ooi '045 nor Ooi '787 teach two host ports having respective task files and a third port having a device task file, an arbitration and control circuit, as recited in claims 1, 9 and 14.

SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA

SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA does not disclose "an arbitration and control circuit … responsive to the original queue depth value and operative to alter the original queue depth value into a queue depth value that is less than the original queue depth value ….", as in the claimed invention. Nor does SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA disclose the "concurrency" of the claimed invention.

The combination of references do not teach, suggest, or hint each and every element of the claimed invention

It is understood, as confirmed by the Examiner during a conversation on July 8, 2008 and noted in an Interview Summary regarding US Application No. 10/775,488, dated 7/18/2008 that the first and second host task files of the claimed invention are presumed to be the task file queue of Utsunomiya, shown in Fig. 4 of Utsunomiya and the claimed device task file is presumed to be the task file shown in Fig. 5 of Utsunomiya. It also appears from the statements made in the office action that the task file queue of Utsunomiya is being doubled and each placed into the host port of Grieff. It is submitted that such a design, as disclosed by Utsunomiya and Grieff will not work because among other reasons, the task file queues of Utsunomiya Operate in a different layer and in accordance with a different protocol than that of Grieff. The backward compatibility feature of Ooi '045/'787 does not make this combination work either because the pieces of the puzzle will not fit!

Utsunomiya's task file queue is not in a SATA port or any port that is responsive to a host, such as in the claimed invention, rather, it is in the main memory 16 of the host because the main memory 16 is coupled to the CPU 14 and the combination form a host or at least a part thereof.

Ooi '045 and Ooi '787, individually or in combination with Grieff and Utsunomiya, do not disclose, suggest, hint at or teach the claimed invention

Due to the recent addition of Ooi '045 and Ooi '787 to the combination of references forming the basis of this rejection, a brief overview of these two references is now presented.

Ooi '045 discloses a computer system 100 including a processor 110, serial ATA (SATA) devices 176 and 178 and an ATA controller 155. The controller 155 includes an emulator for

backward compatibility with parallel ATA (PATA) device drivers, in particularly PATA drivers 138 and 145. [See Ooi '045: Figs. 2 and 3; Col. 2, lines 22-30; Col. 3, lines 23 – 27]. The processor 110 is a central processor unit. [See Ooi '045; Col. 2, lines 31 – 39.]

Ooi '045 discloses a technique to emulate or mimic parallel ATA (PATA) interface in a SATA environment. [See Ooi '045: Col. 1, lines 41-43; Col. 4, lines 49 -55.] To mimic PATA interface, Ooi '045 discloses an elaborate structure to emulate PATA including the emulator 210, the input/output controller hub (ICH) 150, and the parallel ATA drivers 138 and 145. This is done by modifying software drivers for PATA to accommodate SATA. PATA emulation, in the manner used in Ooi '045, allows the PATA driver 138 to control the SATA devices 176 and 178 as if the latter were PATA devices and when the emulator 210 is disabled, the SATA devices 176 and 178 are treated as they are, SATA devices. [See Ooi '045: Col. 4, lines 60 -67.] The serial port 1 task files 225 and the serial task file 235 are in communication with a respective SATA device 1 and 2 [See Ooi '045: Figs. 1 and 2].

Ooi '787 discloses a method and system for updating files including transmitting a frame having status information and non-status information between a device and a host controller. [See Ooi '787: Col. 1, lines 40 - 42.] Ooi '787 appears to be cited for the notion of backward compatibility, however, such compatibility does not suggest that including a hardware structure of one protocol into hardware of another protocol will work. The only backward compatibility disclosed by both Ooi '045 and '787 is modification of software drivers/programs to fool the hardware into thinking that it is PATA. However, to fool the hardware of Utsunomiya using the scheme of the Ooi references, which appears to be suggested as the basis of the foregoing rejection, would require substantial re-design of Utsunomiya and Grieff, if it can be done at all, not to mention the uncertainty as to the incorporation of any of Ooi's structures into the mix.

More specifically, it appears that in the office action, the backward compatibility of SATA with PATA interfaces in Ooi '045 and a paragraph in Ooi '787 are being relied upon to form the conclusion that Utsunomiya's task file queue may be included in the SATA host ports of Grieff. To follow this notion, one would have to import practically all of the structures of Figs. 1 and 2 of Ooi '045 and double the same and use each to couple to a task file queue of Utsunomiya and then to include all of foregoing into each of the host ports 130 and 132 of Grieff. This would clearly result in a system with an exorbitant amount of circuitry, if it works at

all. That is, at least the structures emulator 210, serial ATA host controller 220, serial ATA host controller 230, and the remainder of ICH150, parallel ATA driver 138, parallel ATA driver 145, would have to be made to somehow connect and work with the task file queue of Utsunomiya and placed somehow into the host port 130 or 132 of Grieff and the same done with the other host port of Grieff, which, at the very least, is impractical and inoperational and not at all obvious. In fact, such a combination makes for, if it works at all, such complicated circuitry that this notion by itself welcomes the claimed invention as a marked improvement thereover due to its simplicity of design and therefore much needed.

The task file queue of Utsunomiya, as disclosed, is in the main memory 16 thereof and in communication with a CPU not the SATA devices (drives) as disclosed in Ooi '045. If the serial port 1 task file 225 and the serial port 2 task file 235 of Ooi '045 were to replace the task file queue of Utsunomiya., it is not clear where the task file of Utsunomiya would have to be and how would it would work with the structures of Ooi '045.

Thus, Utsunomiya and Ooi '045 and Ooi '787 combined with Grieff fail to disclose the claimed arbitration and control circuit.

None of the references, either individually or in combination, disclose or teach SATA ports responsive to non-data FIS from the host unit, as in the claimed invention.

None of the references, either individually or in combination, disclose or teach "an arbitration and control circuit … responsive to the original queue depth value and operative to alter the original queue depth value into a queue depth value that is less than the original queue depth value ….", as in the claimed invention. To the contrary, in Grieff, an error would occur when the queue depth is exceeded, which would not happen in the claimed invention. [See Grieff: Fig. 2, note on the bottom left-side of the page, starting with "Don't forward the Queued command to the Device if the Task Queue is full. Make it look like the device had an error …."] In accordance with the claimed invention, the task queue would never become full because the host units are fooled into believing that the queue depth is less than its actual size.

Applicants thus submit that the cited combination lacks at least one element of the claimed invention, and that any combination will not work without re-engineering the art beyond recognition.

The claimed invention is not obvious because the cited combination of references forming the basis of rejection simply does not work

Combining Utsunomiya's task file queue (TFQ) into Grieff's ATA ports using some of the circuits shown in Ooi '045 does not work.

The host ports 130 and 132 in Grieff are state machines for relaying primitives with no mention of storage capability. [See: Grieff: Col. 5, lines 50-56]. Indeed, if the capability existed in Grieff's host ports 130 and 132 to store commands or non-data FIS, arguably Grieff would not have needed to store and decode host commands after the switch, i.e. FIS buffer 120.

Furthermore, the host ports 130 and 132 in Grieff operate at the Link Layer (layer 2). In comparison, the TFQs from Utsunomiya function in PATA protocol, which is basically an Application Layer.

Thus, the link layer host ports 130 and 132 of Grieff, lacking storage capability, can neither store nor interface with the application layer TFQs from Utsunomiya. To use some of the circuitry disclosed in Ooi '045, particularly the emulator 210, serial ATA host controller 220, serial ATA host controller 230, and the remainder of ICH150, parallel ATA driver 138, parallel ATA driver 145, to cause backward compatibility of the host ports 130 and 132 of Grieff and the task file queue of Utsunomiya would require an impractical circuit/structure. Notwithstanding the foregoing, it is not clear and certainly not disclosed in the proposed combination, where and how such circuits would be located and connected.

Furthermore, the arbiter module 112 of Grieff processes at the Link Layer (layer 2) rather than the command layer (layer 4). [See: Grieff, Col. 5, Lns. 50-56]. Redesigning the arbiter module 112 would in turn require re-engineering each subsequent component to interact with command layer (layer 4) at the host ports 130, 132. Without redesigning each subsequent component the system simply would not work.

Neither Ooi '045 nor Ooi '787 offer guidance to this effect, as they both disclose modifying drivers/programs to mimic PATA where SATA devices are employed. It is not clear how such an emulation technique would be designed into Utsunomiya and then carried over to Grieff without redesigning all three systems.

In short, simply "including" Utsunomiya's TFQs into Grieff's ATA ports using the disclosure of Ooi '045 and '787 will not work because at least the following sub-systems will need to be re-engineered or eliminated:

- The ports 130, 132 in Grieff. As recited, these ports don't have storage capability to handle TFQs.
- Utusunomiya's TFQ 22. As recited, the TFQ 22 is "done in software" and resides in RAM 16. Furthermore, it functions in PATA, and is not compatible with SATA FIS.
- Grieff's OR Table 116. If routing of non-data FIS were transparent to the switch, much of the functionality of this sub-system would be rendered useless, but it's unclear that the OR Table could simply be removed.
- Grieff's decoder 120. Much of the functionality of this sub-system would be rendered useless by the TFQs, but it's unclear that the decoder could simply be removed.
- Grieff's decoder command tracker SM 114. This state machine accepts and generates control signals for numerous sub-systems that have to be re-engineered or eliminated. Therefore, Figs. 2 through 8 in Grieff, showing the various states in the command tracker state machine 114, would have to be substantially re-engineered.

That is, for the foregoing reasons, among others, the TFQs of Utsunomiya *cannot* simply be inserted into the host ports of Grieff even using the emulation technique of Ooi '045 and '787.

Any combination of these elements would require, if can be done at all, re-engineering to such an extent as to render them practically unrecognizable.

Applicants thus submit that the cited combination lacks an element of the claimed invention, and that any combination will not work without re-engineering the art beyond recognition.

The claimed invention is not obvious because the combination does not disclose, suggest, hint at or teach "selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time"

Because the combination of references does not work, it necessarily lacks the foregoing concurrency limitation.

Applicants thus submit that the cited combination lacks an element of the claimed invention, and that any combination will not work without re-engineering the art beyond recognition.

Regarding claims 5-17, 19, 23-30, 32, 36-43, they are necessarily allowable as they depend from allowable independent claims.

Reconsideration and allowance of claims 1, 5-19, 23-32, and 36-45 is hereby respectfully requested. Consideration and allowance of claims 44-45 is respectfully requested. Applicants submit that the subject application is now in condition for allowance and an early notice thereof is respectfully requested. Should any further amendment be required prior to passing the application to issue, the Examiner is respectfully invited to contact the undersigned by telephone at the number set out below.

Respectfully submitted,
LAW OFFICES OF IMAM

Dated: September 23, 2008
By ____/maryam imam/_____
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I hereby certify that this correspondence with all attachments is being electronically filed with the United States Patent and Trademark Office: Mail Stop No Fee Amendment, Commissioner for Patents, P.O. Box 1450, Arlington VA 22313-1450 on September 23, 2008 by Maryam Imam.

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